the duration of the pulse and the voltage source is disconnected before the pulse has time to propagate through the circuit attached to said output.

A2

4. (Amended) A method according to [any of claims 1 to 4] claim 1, further comprising the steps of:

applying a voltage to said input, which is applied to said output via the relatively high resistance to apply a test voltage having a weak drive strength to the output.

A3

6. (Amended) A method according to [any one of claims 1 to 5] claim 1, in which said [analogue] analog model is stimulated with an expanded standard logic package.

A4

8. (Amended) A method according to [any preceding] claim 1, in which said relatively high resistance has a resistance of between 500 kilo ohms and 1.5 mega ohms.

9. (Amended) A method according to [any preceding] claim 1, wherein said relatively low resistance has a resistance of between 0.5 ohms and 10 ohms.

10. (Amended) A method according to [any one of claims 1 to 9] claim 1, in which said pulse has a duration of between 50 pico seconds to 150 pico seconds.

11. (Amended) A method as claimed in [any preceding] claim 1, wherein said [analogue] analog model is a SPICE model.

12. (Amended) A system for reducing delays in an [analogue] analog simulation model of the hardware circuit comprising:

means for stimulation via an input an output of the [analogue] analog model, said output and said input having a relatively high resistance therebetween; and

means for applying a pulse to a relatively low resistance, whereby when said pulse is applied to the relatively low resistance, the input is connected to said output via the relatively low resistance so that the time constant of the circuit is reduced.